

- Digital Design Avoids Analog Compensation Errors
- Easily Cascadable for Higher Order Loops
- Useful Frequency from DC to:
50 MHz Typical (K Clock)
35 MHz Typical (I/D Clock)

description

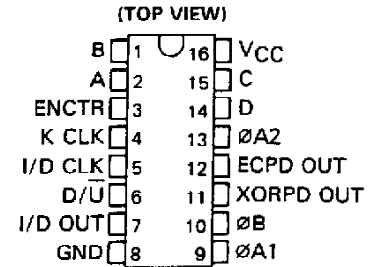
The SN54LS297 and SN74LS297 devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-N counter, to build first order phase-locked loops as described in Figure 1.

Both exclusive-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

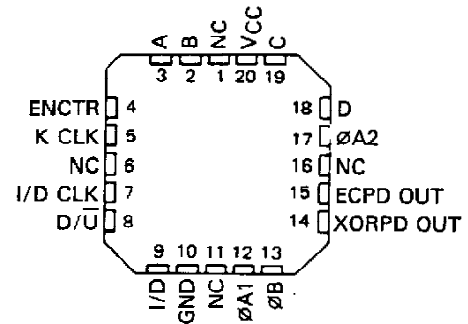
Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C, and D are all programmed high, the K counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

SN54LS297 . . . J OR W PACKAGE
SN74LS297 . . . N PACKAGE



SN54LS297 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

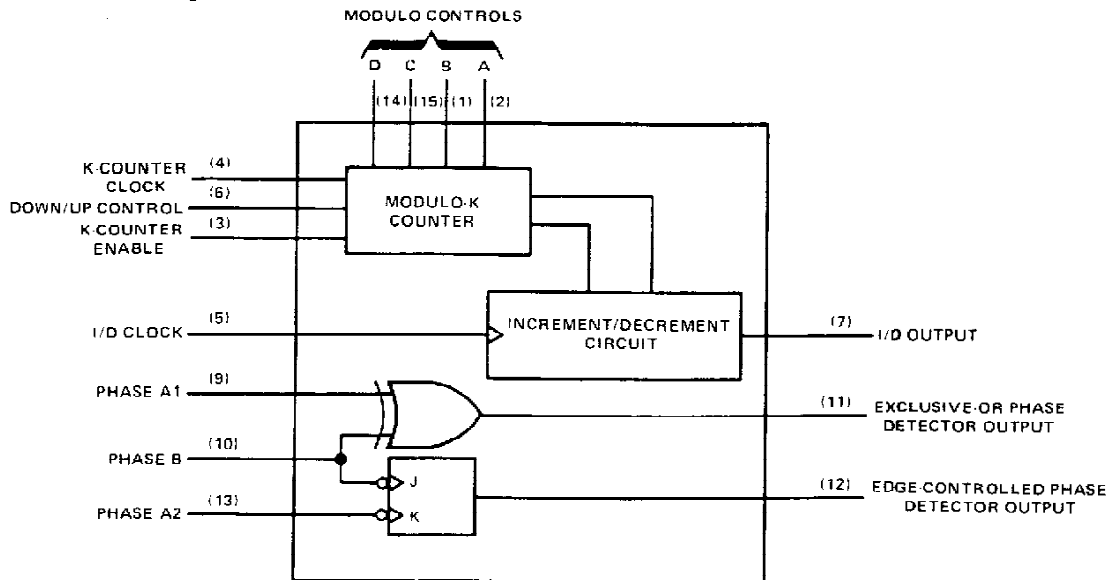


FIGURE 1—SIMPLIFIED BLOCK DIAGRAM

Pin numbers shown are for J, N and W packages.

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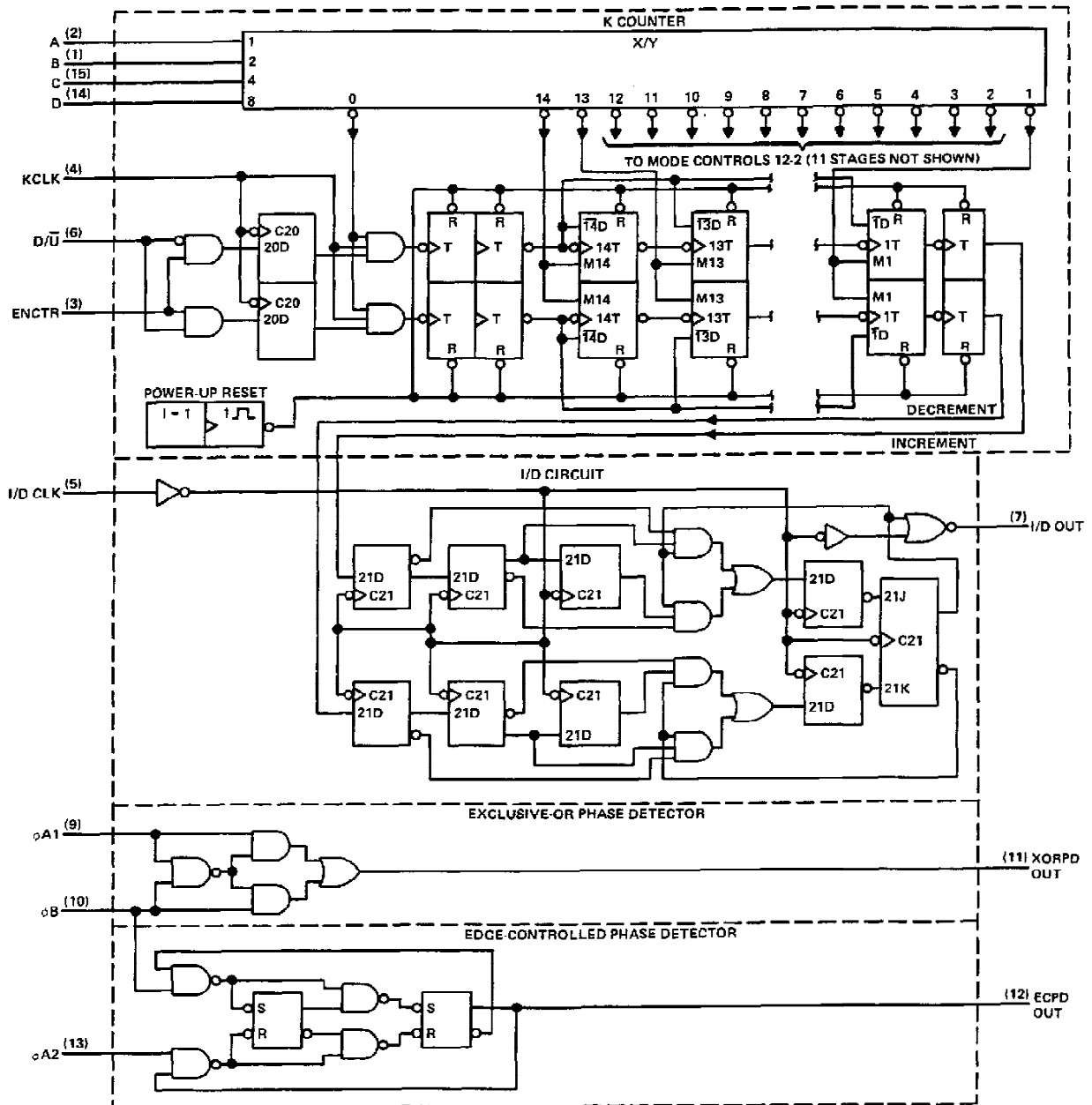


SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

description (continued)

The 'LS297 can perform the classic first-order phase-locked loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock, I/D clock, and loop propagation delays. The I/D clock frequency and the divide-by-N modulus will determine the center frequency of the DPLL. The center frequency is defined by the relationship $f_c = I/D \text{ Clock}/2N$ (Hz).

logic diagram (positive logic)



Pin numbers shown are for J, N, and W packages.

SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

**K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)**

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2 ³
L	L	H	L	2 ⁴
L	L	H	H	2 ⁵
L	H	L	L	2 ⁶
L	H	L	H	2 ⁷
L	H	H	L	2 ⁸
L	H	H	H	2 ⁹
H	L	L	L	2 ¹⁰
H	L	L	H	2 ¹¹
H	L	H	L	2 ¹²
H	L	H	H	2 ¹³
H	H	L	L	2 ¹⁴
H	H	L	H	2 ¹⁵
H	H	H	L	2 ¹⁶
H	H	H	H	2 ¹⁷

**FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR**

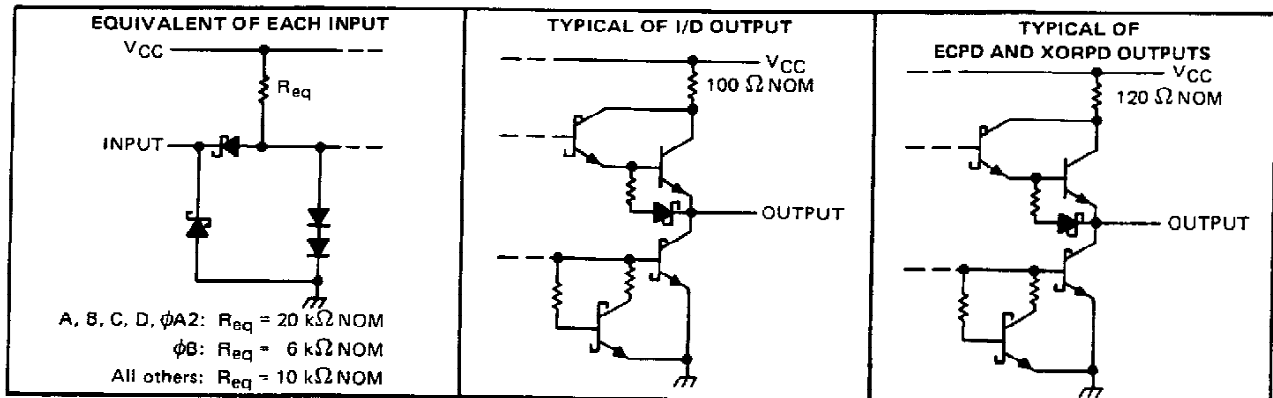
$\phi A1$	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

**FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR**

$\phi A2$	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

schematics of inputs and outputs



operation

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain k_d , which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{PD Output} = \frac{\% \text{ high} - \% \text{ low}}{100} \quad (1)$$

The output of the phase detector will be $k_d \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

Exclusive-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. k_d for an XORPD is 4 because its output remains high (PD output = 1) for a phase error of 1/4 cycle. Similarly, k_d for the ECPD is 2 since its output remains high for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for ϕ_e defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase detector output is a square wave. The XORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are 1/2 cycle out of phase.

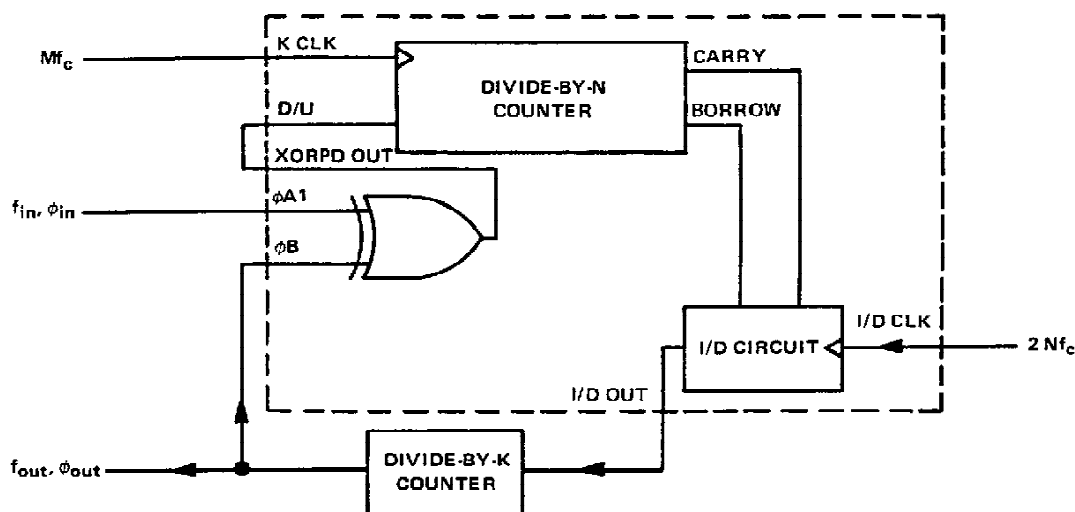


FIGURE 2—DPLL USING EXCLUSIVE-OR PHASE DETECTION

The phase detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_c , which is a multiple M of the loop center frequency f_c . When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_c/K , the output of the K counter will equal the input frequency multiplied by the division ratio. Thus the output from the K counter is $(k_d \phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock I/D CLK. The input clock is just a multiple, $2N$, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D OUT. Thus the output of the I/D circuit will be $Nf_c + (k_d \phi_e Mf_c)/2K$.

The output of the N counter (or the output of the phase-locked loop) is thus:

$$f_o = f_c + (k_d \phi_e Mf_c)/2KN$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for $M = 2N$.

Thus the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

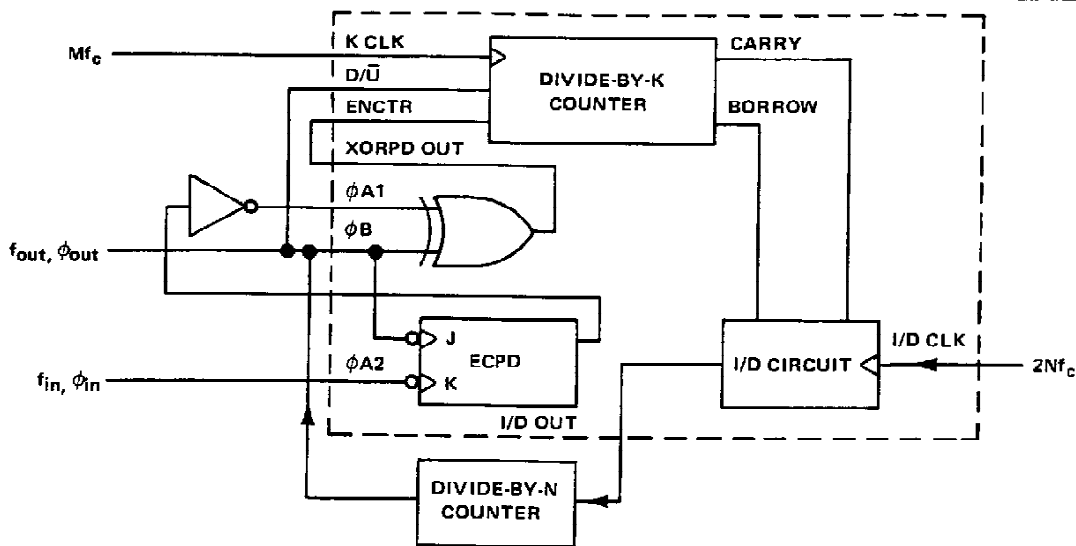


FIGURE 3—DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS297	-55°C to 125°C
SN74LS297	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS297			SN74LS297			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	I/D OUT		-1.2	-1.2		mA	
		EXOR, ECPD		-400	-400		μ A	
I_{OL}	Low-level output current	I/D OUT		12	24		mA	
		XOR, ECPD		4	8		mA	
f_{clock}	Clock frequency	K Clock		0	32		MHz	
		I/D Clock		0	16		MHz	
t_w	Width of clock input pulse	K Clock		16	16		ns	
		I/D Clock		33	33		ns	
$t_{su, to K}$	Setup time to K Clock t	U/D, ENCTR		30	30		ns	
t_h	Hold time from K Clock t	U/D, ENCTR		0	0		ns	
T_A	Operating free-air temperature	-55	125	0	70	°C		



SN54LS297, SN74LS297

DIGITAL PHASE-LOCKED-LOOP FILTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS297			SN74LS297			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	I/D OUT	V _{CC} = MIN, V _{IH} = 2 V,	I _{OH} = MAX	2.4		2.4		V
	Others	V _{IL} = V _{IL} max	I _{OH} = MAX	2.5		2.7		
V _{OL} Low-level output voltage	I/D OUT	V _{CC} = MIN, V _{IH} = 2 V,	I _{OL} = 12 mA		0.25	0.4		V
			I _{OL} = 24 mA				0.35	
	Others	V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25	
			I _{OL} = 8 mA			0.35	0.5	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V					0.1		mA
I _{IH} High-level input current	U/D, EN, φA1	V _{CC} = MAX, V _I = 2.7 V			40		40	μA
	φB				60		60	
	All others				20		20	
I _{IL} Low-level input current	U/D, EN, φA1	V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8	mA
	φB				-1.2		-1.2	
	All others				-0.4		-0.4	
I _{OS} Short-circuit output current §	I/D OUT	V _{CC} = MAX		-30	-130		-30	mA
	Others			-20	-100		-20	
I _{CC} Supply current	V _{CC} = MAX, All inputs grounded, All outputs open		75	120		75	120	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are of V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	KCLK	I/D OUT	R _L = 667 Ω, C _L = 45 pF, See Note 2	32	50		MHz
	I/D CLK †	I/D OUT		16	35		
t _{PLH}	I/D CLK †	I/D OUT		15	25		ns
t _{PHL}	I/D CLK †	I/D OUT		22	35		ns
t _{PLH}	φA1 or φB	Other input low	R _L = 2 kΩ, C _L = 45 pF, See Note 2	10	15		ns
	φA1 or φB	Other input high		17	25		
t _{PHL}	φA1 or φB	Other input low		15	25		ns
	φA1 or φB	Other input high		17	25		
t _{PLH}	φB ↓	ECPD OUT		20	30		ns
t _{PHL}	φA2 ↓	ECPD OUT		20	30		ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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