FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4046BC
Micropower Phase-Locked Loop

General Description

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic power consumption: 70 μW (typ.) at f_o = 10 kHz, V_{DD} = 5V
- VCO frequency: 1.3 MHz (typ.) at V_{DD} = 10V
- Low frequency drift: 0.06%/°C at V_{DD} = 10V with temperature
- High VCO linearity: 1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

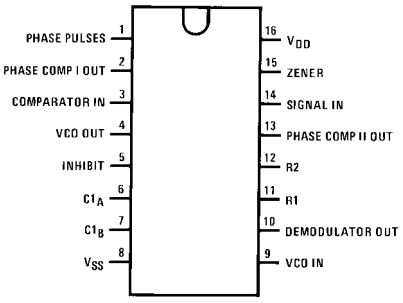
Ordering Code:

Order Number	Package Number	Package Description
CD4046BCM	M16A	16-Lead Small Outline integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4046BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for SOIC and DIP



Top View

Block Diagram

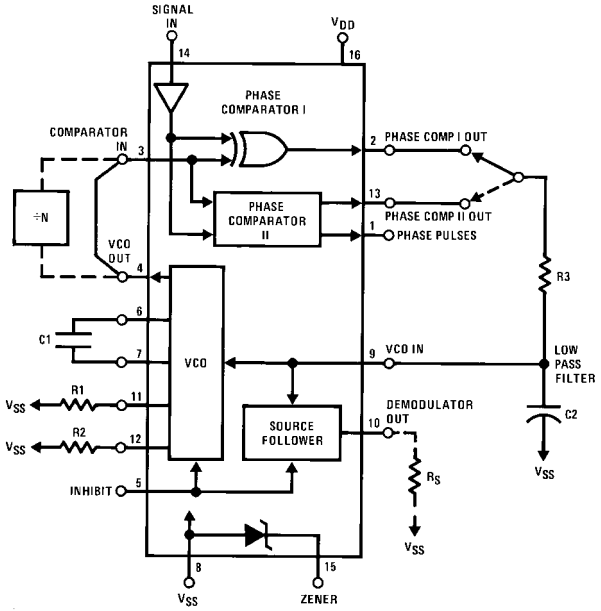


FIGURE 1.

Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD},								
		Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	µA
		V_{DD} = 10V		40		0.01	40		300	µA
		V_{DD} = 15V		80		0.015	80		600	µA
		Pin 5 = V_{DD}, Pin 14 = Open,								
		Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	µA
		V_{DD} = 10V		530		20	410		710	µA
		V_{DD} = 15V		1500		50	1200		1800	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	Comparator and Signal In	V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	Comparator and Signal In	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 4)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 4)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA
C_{IN}	Input Capacitance	Any Input (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ,								
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCO SECTION						
I_{DD}	Operating Current	f_o = 10 kHz, R1 = 1 MΩ,				
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}/2$				
		V_{DD} = 5V		20		µA
		V_{DD} = 10V		90		µA
		V_{DD} = 15V		200		µA
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF, R1 = 10 kΩ,				
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}$				
		V_{DD} = 5V	0.4	0.8		MHz
		V_{DD} = 10V	0.6	1.2		MHz
		V_{DD} = 15V	1.0	1.6		MHz
	Linearity	VCO_{IN} = 2.5V ±0.3V,				
		R1 ≥ 10 kΩ, V_{DD} = 5V		1		%
		VCO_{IN} = 5V ±2.5V,				
		R1 ≥ 400 kΩ, V_{DD} = 10V		1		%
		VCO_{IN} = 7.5V ±5V,				
		R1 ≥ 1 MΩ, V_{DD} = 15V		1		%
	Temperature-Frequency Stability	%/°C∝1/ϕ. $\varsigma_{\Delta\Delta}$				
	No Frequency Offset, $f_{MIN} = 0$	R2 = ∞				
		V_{DD} = 5V		0.12–0.24		%/°C
		V_{DD} = 10V		0.04–0.08		%/°C
		V_{DD} = 15V		0.015–0.03		%/°C
	Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
		V_{DD} = 10V		0.05–0.1		%/°C
		V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN}	Input Resistance	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
VCO	Output Duty Cycle	V_{DD} = 5V		50		%
		V_{DD} = 10V		50		%
		V_{DD} = 15V		50		%
t_{THL}	VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		45	80	ns
PHASE COMPARATORS SECTION						
R_{IN}	Input Resistance					
	Signal Input	V_{DD} = 5V	1	3		MΩ
		V_{DD} = 10V	0.2	0.7		MΩ
		V_{DD} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
	AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF				
		f = 50 kHz				
		V_{DD} = 5V		200	400	mV
		V_{DD} = 10V		400	800	mV
		V_{DD} = 15V		700	1400	mV

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DEMODULATOR OUTPUT						
$VCO_{IN}-V_{DEM}$	Offset Voltage	RS ≥ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
		RS ≥ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
		RS ≥ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
	Linearity	RS ≥ 50 kΩ				
		VCO_{IN} = 2.5V ±0.3V, V_{DD} = 5V		0.1		%
		VCO_{IN} = 5V ±2.5V, V_{DD} = 10V		0.6		%
		VCO_{IN} = 7.5V ±5V, V_{DD} = 15V		0.8		%
ZENER DIODE						
V_Z	Zener Diode Voltage	I_Z = 50 µA	6.3	7.0	7.7	V
R_Z	Zener Dynamic Resistance	I_Z = 1 mA		100		Ω

Note 5: AC Parameters are guaranteed by DC correlated testing.

Phase Comparator State Diagrams

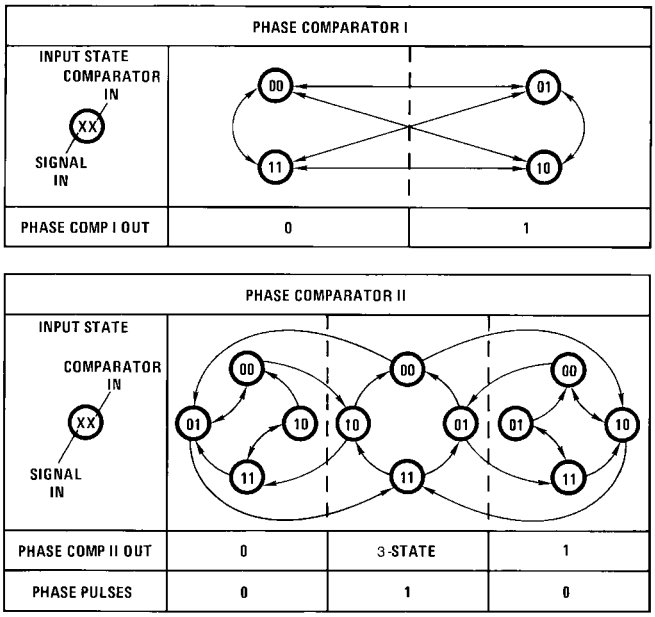


FIGURE 2.

Typical Waveforms

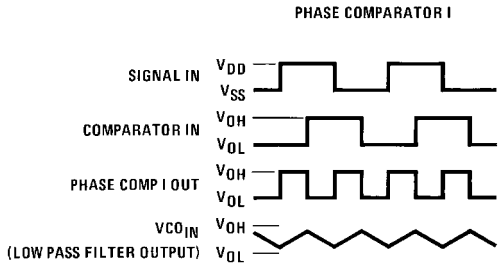


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

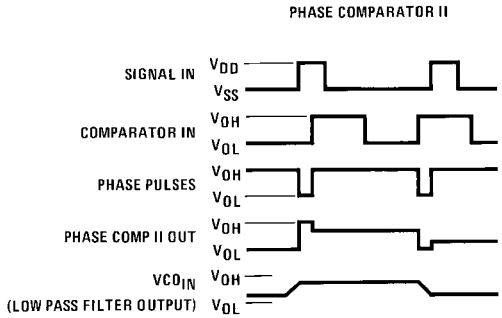


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

Typical Center Frequency vs C1
for R1 = 10 kΩ, 100 kΩ and 1 MΩ

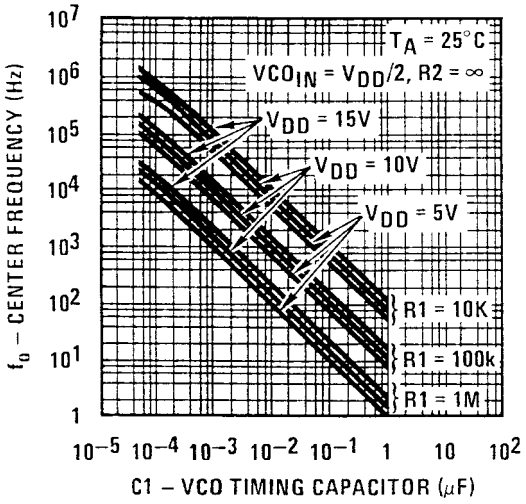


FIGURE 5.

Typical Frequency vs C1
for R2 = 10 kΩ, 100 kΩ and 1 MΩ

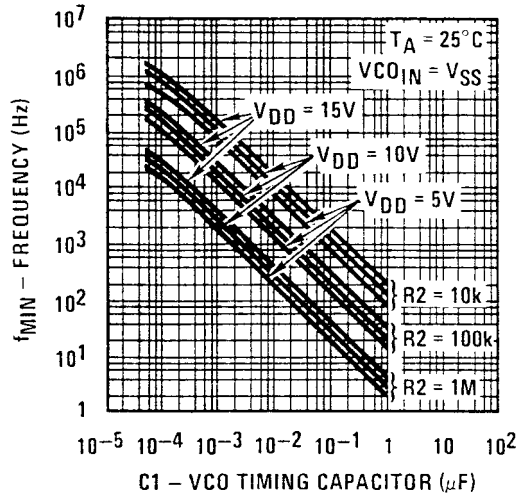


FIGURE 6.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical f_{MAX}/f_{MIN} vs R2/R1

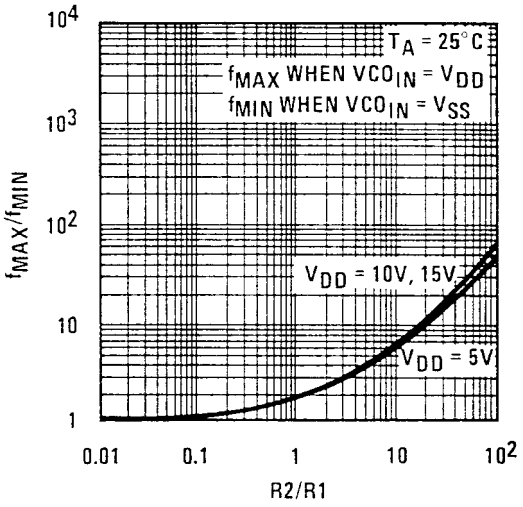


FIGURE 7.

Typical VCO Power Dissipation at Center Frequency vs R1

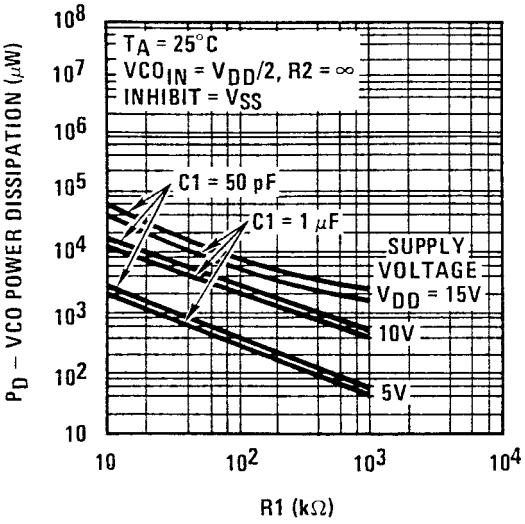


FIGURE 8.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical VCO Power Dissipation at f_{MIN} vs R2

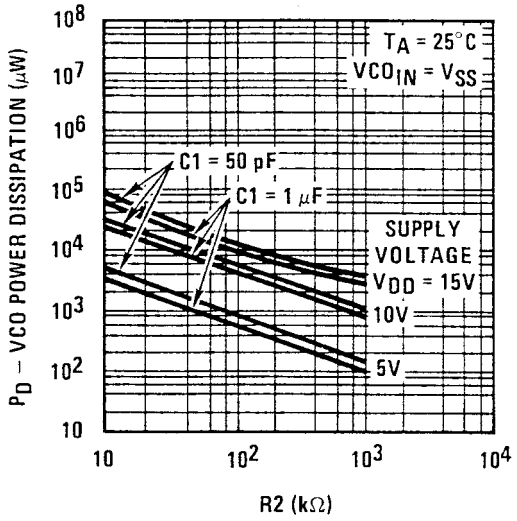


FIGURE 9.

Typical Source Follower Power Dissipation vs R_S

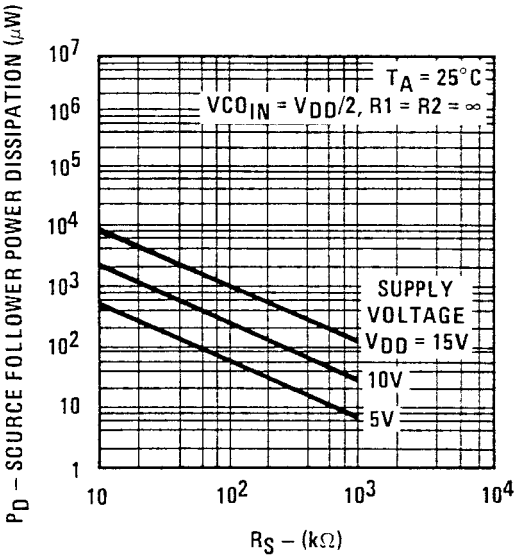


FIGURE 10.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

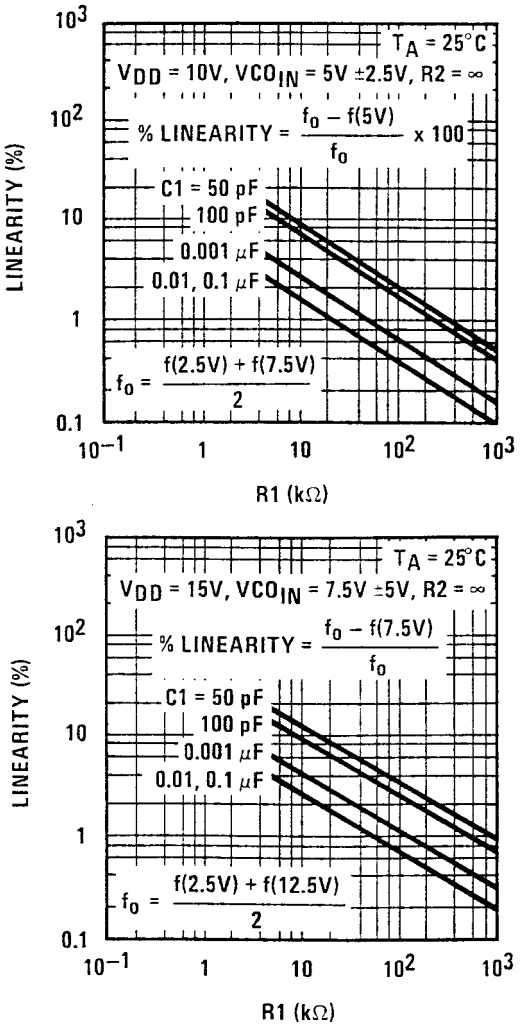


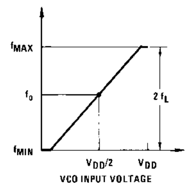
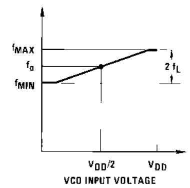
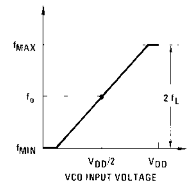
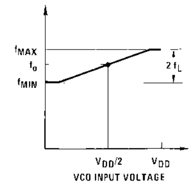
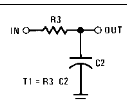
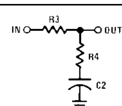
FIGURE 11. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 ≥ 10 kΩ, R_S ≥ 10 kΩ, C1 ≥ 50 pF.

In addition to the given design information, refer to Figure 5, Figure 6, Figure 7 for R1, R2 and C1 component selections.

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	**VCO With Offset**	**VCO Without Offset R2 = ∞**	**VCO With Offset**
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, 2 f_L	2 f_L = full VCO frequency range 2 f_L = f_{max} – f_{min}			
Frequency Capture Range, 2 f_C		$2 f_C \approx \frac{1}{\pi}\sqrt{\frac{2 \pi f_L}{\tau 1}}$	$f_C = f_L$	
Loop Filter Component Selection		For 2 f_C, see Ref.		
Phase Angle Between Single and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

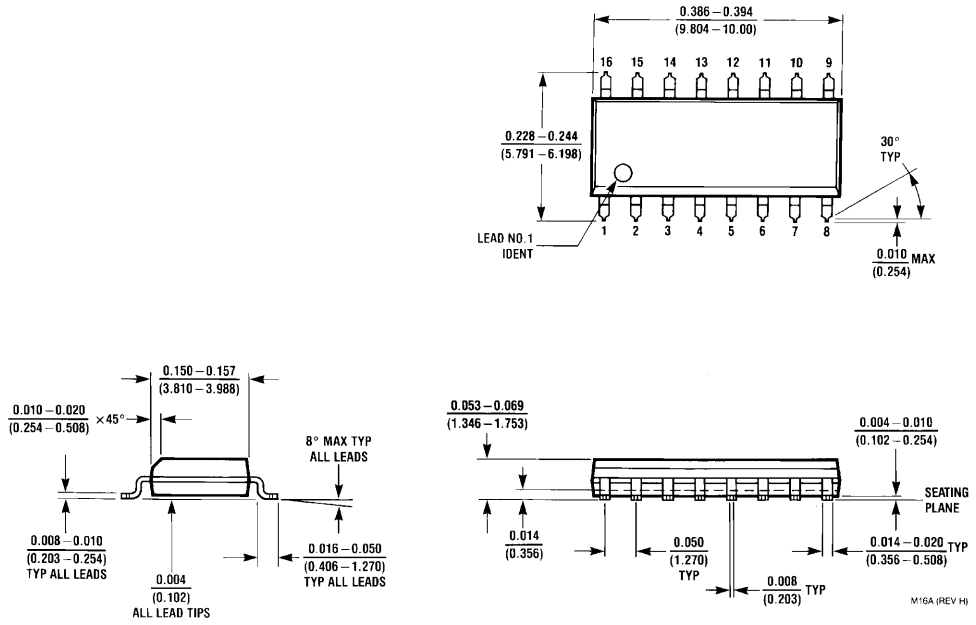
Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset **R2** = ∞	VCO With Offset	VCO Without Offset **R2** = ∞	VCO With Offset
VCO Component Selection	Given: f_o. Use f_o with Figure 5 to determine R1 and C1.	Given: f_o and f_L. Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with Figure 6 to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$. Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.	Given: f_{max}. Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$. Use f_o with Figure 5 to determine R1 and C1.	Given: f_{min} and f_{max}. Use f_{min} with Figure 6 to to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.

References

G.S. Moschytz, “Miniaturized RC Filters Using Phase-Locked Loop”, BSTJ, May, 1965.

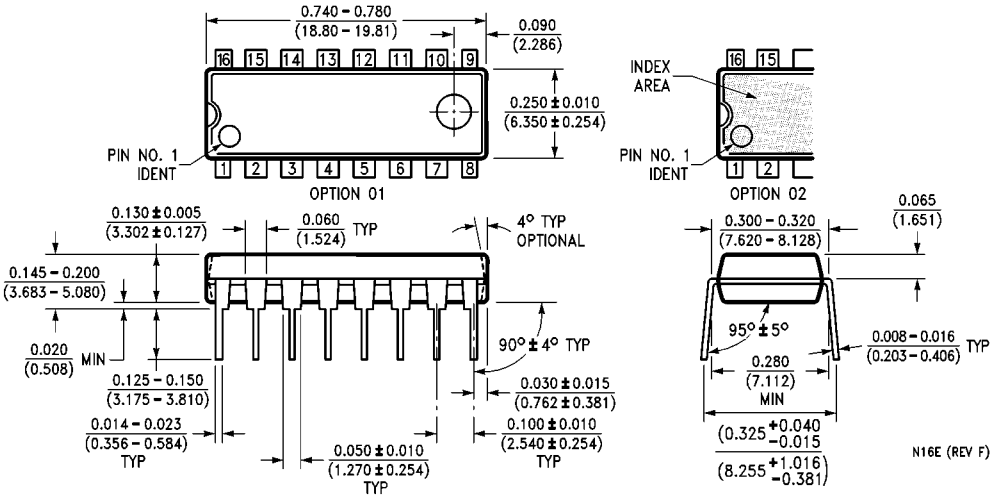
Floyd Gardner, “Phaselock Techniques”, John Wiley & Sons, 1966.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com